IN THE CLAIMS:

1. (Currently Amended) A method, comprising:

forming a recessed first sidewall spacer adjacent to a sidewall of a polysilicon line formed above a substrate, said first sidewall spacer exposing an upper sidewall portion of said polysilicon line;

forming a second sidewall spacer comprised of silicon dioxide adjacent to said first sidewall spacer, said second sidewall spacer having a predefined etch selectivity with respect to said polysilicon line and said substrate, wherein forming said second sidewall spacer includes depositing a silicon dioxide layer over said polysilicon line and said first recessed sidewall spacer and anisotropically etching said silicon dioxide layer, whereby an etch chemistry is selective to silicon;

reducing a size of said second sidewall spacer by a selective etch process according to said predefined etch selectivity so as to expose at least said upper sidewall portion; and

forming a metal silicide region at least on said exposed upper sidewall portion.

2. (Original) The method of claim 1, wherein forming said recessed first sidewall spacer includes:

forming a conformal silicon dioxide layer on said polysilicon line;

depositing a silicon nitride layer over said polysilicon line; and

anisotropically etching said silicon nitride layer until said upper sidewall portion is exposed.

3. (Original) The method of claim 1, wherein said second sidewall spacer is comprised of silicon dioxide.

4. (Canceled)

5. (Currently Amended) The method of ~~claim 4~~ claim 1, further comprising performing a selective isotropic etch process to remove silicon dioxide prior to forming said metal silicide region, wherein said upper sidewall portion is substantially completely exposed.

6. (Original) The method of claim 5, further comprising forming doped regions adjacent to the polysilicon line.

7. (Original) The method of claim 6, wherein said first and second sidewall spacers are used as implantation masks during the formation of said doped regions.

8. (Original) The method of claim 6, further comprising forming metal silicide regions in said doped regions substantially at the same time when forming said metal silicide region in said polysilicon line.

9. (Original) The method of claim 8, wherein a lateral extension of said metal silicide regions in said doped regions is adjusted by controlling silicon dioxide removal during said selective etch process for reducing the size of said second sidewall spacer.

10. (Currently Amended) A method, comprising:

forming a silicon dioxide liner on sidewalls of a polysilicon line formed above a silicon region;

forming a recessed first sidewall spacer on said silicon dioxide liner, said first sidewall spacer being comprised of a material that may be selectively etched with respect to silicon dioxide;

forming a silicon dioxide sidewall spacer adjacent to said first sidewall spacer; and

selectively removing said silicon dioxide layer at least on portions of said polysilicon line not covered by said first sidewall spacer.

11. (Currently Amended) The method of claim 10, wherein forming a silicon dioxide sidewall spacer includes depositing a silicon dioxide layer and partially removing silicon dioxide by an anisotropic etch process.

12. (Original) The method of claim 11, wherein said anisotropic etch process is selective with respect to silicon and said anisotropic etch process is performed to expose an upper portion of said polysilicon line.

13. (Original) The method of claim 10, wherein selectively removing silicon dioxide includes substantially completely removing silicon dioxide from a top surface of said polysilicon line, sidewall portions not covered by said first sidewall spacer and surface portions of the silicon region not covered by said first and second sidewall spacers.

14. (Original) The method of claim 13, wherein said selective removal is a selective wet etch process.

15. (Original) The method of claim 14, wherein a lateral extension of the silicon region not covered by said first and second sidewall spacers is adjusted in conformity with a specified target value by controlling said selective wet etch process.

16. (Original) The method of claim 13, wherein a thickness of said dioxide liner is selected so as to enable an at least partial filling in of a refractory metal after completion of said selective wet etch process.

17. (Original) The method of claim 10, further comprising depositing a metal over said polysilicon line and forming a metal silicide at least in portions not covered by said first and second sidewall spacers.

18. (Original) The method of claim 13, further comprising depositing a metal over said polysilicon line and said silicon region and forming a metal silicide on regions that are substantially devoid of silicon dioxide.

19. (Original) The method of claim 10, further comprising forming doped areas of a specified doping profile in said silicon region.

20. (Original) The method of claim 19, wherein at least one of said first and second sidewall spacers acts as a mask for laterally patterning said specified doping profile.

21. (Original) The method of claim 20, wherein said doped areas are formed by ion implantation.

22. (Currently Amended) A method of forming a field effect transistor, the method comprising:

forming a gate electrode on a gate insulation layer above a region, said region being comprised of a specified semiconductive material;

forming a first recessed sidewall spacer, comprising at least a layer of a first dielectric material in contact with said gate electrode, and a second sidewall spacer, said second sidewall spacer being comprised of said first dielectric material, said first dielectric material having a specified etch selectivity with respect to said specified semiconductive material;

forming a drain region and a source region;

selectively removing a portion of said first dielectric material to substantially completely expose an upper sidewall portion of said gate electrode; and

forming a metal/semiconductor compound region in said gate electrode, wherein said exposed upper sidewall portion promotes metal diffusion into said gate electrode, wherein said drain and source regions are substantially completely exposed by an isotropic selective etch process prior to forming said metal/semiconductor compound region.

23. (Original) The method of claim 22, wherein forming said first recessed sidewall spacer includes depositing a layer of material on said layer of first dielectric material and anisotropically etching said layer of material to form said first recessed sidewall spacer.

24. (Currently Amended) The method of ~~claim 23~~ claim 22, wherein forming said second sidewall spacer includes depositing a layer of said first dielectric material and anisotropically etching said first dielectric material, whereby said predefined etch selectivity substantially suppresses an etching of said gate electrode and said drain and source regions.

25. (Original) The method of claim 24, wherein a height of said second sidewall spacer is adjusted by controlling an etch time of said anisotropic etch process.

26. (Canceled)

27. (Currently Amended) The method of ~~claim 26~~ claim 22, wherein said isotropic selective etch process is a wet chemical etch process on the basis of hydrogenated fluoride.

28. (Currently Amended) The method of ~~claim 26~~ claim 22, wherein a lateral extension of a substantially completely exposed area of said drain and source regions is adjusted in conformity with a predefined target value by controlling said isotropic selective etch process.

29. (Original) The method of claim 22, wherein said first dielectric material comprises silicon dioxide.

30. (Currently Amended) The method of ~~claim 29~~ claim 22, wherein said first sidewall spacer is comprised of silicon nitride.

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (New) A method, comprising:

forming a recessed first sidewall spacer adjacent to a sidewall of a polysilicon line formed above a substrate, said first sidewall spacer exposing an upper sidewall

portion of said polysilicon line, wherein forming said recessed first side spacer comprises:

forming a conformal silicon dioxide layer on said polysilicon line;

depositing a silicon nitride layer over said polysilicon line; and

anisotropically etching said silicon nitride layer until said upper sidewall portion is exposed;

forming a second sidewall spacer adjacent to said first sidewall spacer, said second sidewall spacer having a predefined etch selectivity with respect to said polysilicon line and said substrate;

reducing a size of said second sidewall spacer by a selective etch process according to said predefined etch selectivity so as to expose at least said upper sidewall portion; and

forming a metal silicide region at least on said exposed upper sidewall portion.

37. (New) A method of forming a field effect transistor, the method comprising:

forming a gate electrode on a gate insulation layer above a region, said region being comprised of a specified semiconductive material;

forming a first recessed sidewall spacer, comprising at least a layer of a first dielectric material in contact with said gate electrode, and a second sidewall spacer, said second sidewall spacer being comprised of said first dielectric material, said first dielectric material having a specified etch selectivity with respect to said specified semiconductive material, wherein forming said first recessed sidewall spacer includes depositing a layer of material on said layer of first dielectric material and

anisotropically etching said layer of material to form said first recessed sidewall spacer;

forming a drain region and a source region;

selectively removing a portion of said first dielectric material to substantially completely expose an upper sidewall portion of said gate electrode; and

forming a metal/semiconductor compound region in said gate electrode, wherein said exposed upper sidewall portion promotes metal diffusion into said gate electrode.

38. (New) A method of forming a field effect transistor, the method comprising:

forming a gate electrode on a gate insulation layer above a region, said region being comprised of a specified semiconductive material;

forming a first recessed sidewall spacer, comprising at least a layer of a first dielectric material in contact with said gate electrode, and a second sidewall spacer, said second sidewall spacer being comprised of said first dielectric material, said first dielectric material having a specified etch selectivity with respect to said specified semiconductive material, wherein forming said second sidewall spacer includes depositing a layer of said first dielectric material and anisotropically etching said first dielectric material, whereby said predefined etch selectivity substantially suppresses an etching of said gate electrode and said drain and source regions;

forming a drain region and a source region;

selectively removing a portion of said first dielectric material to substantially completely expose an upper sidewall portion of said gate electrode; and

forming a metal/semiconductor compound region in said gate electrode, wherein said exposed upper sidewall portion promotes metal diffusion into said gate electrode.

39. (New) The method of claim 38, wherein a height of said second sidewall spacer is adjusted by controlling an etch time of said anisotropic etch process.

40. (New) A method of forming a field effect transistor, the method comprising:

forming a gate electrode on a gate insulation layer above a region, said region being comprised of a specified semiconductive material;

forming a first recessed sidewall spacer comprised of silicon nitride, comprising at least a layer of a first dielectric material in contact with said gate electrode, and a second sidewall spacer, said second sidewall spacer being comprised of said first dielectric material, said first dielectric material having a specified etch selectivity with respect to said specified semiconductive material;

forming a drain region and a source region;

selectively removing a portion of said first dielectric material to substantially completely expose an upper sidewall portion of said gate electrode; and

forming a metal/semiconductor compound region in said gate electrode, wherein said exposed upper sidewall portion promotes metal diffusion into said gate electrode.